FIG. 1

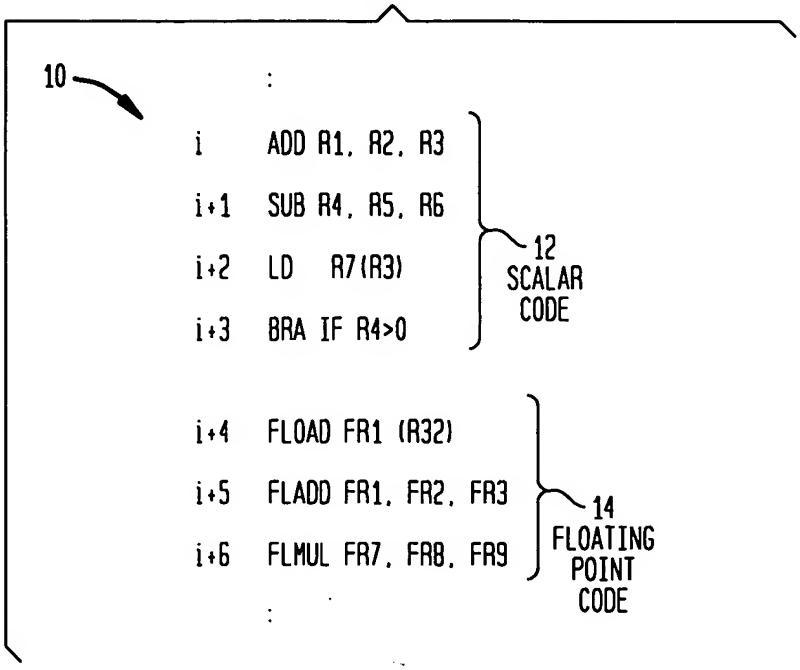

10
:
i ADD R1, R2, R3
i+1 SUB R4, R5, R6
i+2 LD R7(R3)
i+3 BRA IF R4>0
12
SCALAR CODE
i+4 FLOAD FR1 (R32)
i+5 FLADD FR1, FR2, FR3
i+6 FLMUL FR7, FR8, FR9
14
FLOATING POINT CODE
:

FIG. 2

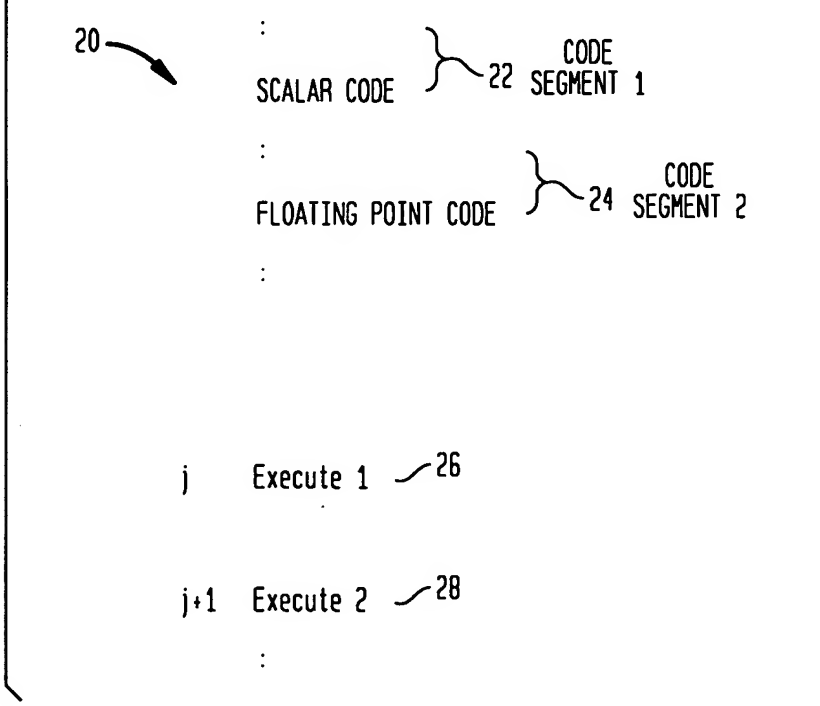

20
:
SCALAR CODE
22
CODE SEGMENT 1
:
FLOATING POINT CODE
24
CODE SEGMENT 2
:
j Execute 1
26
j+1 Execute 2
28
:

FIG. 3

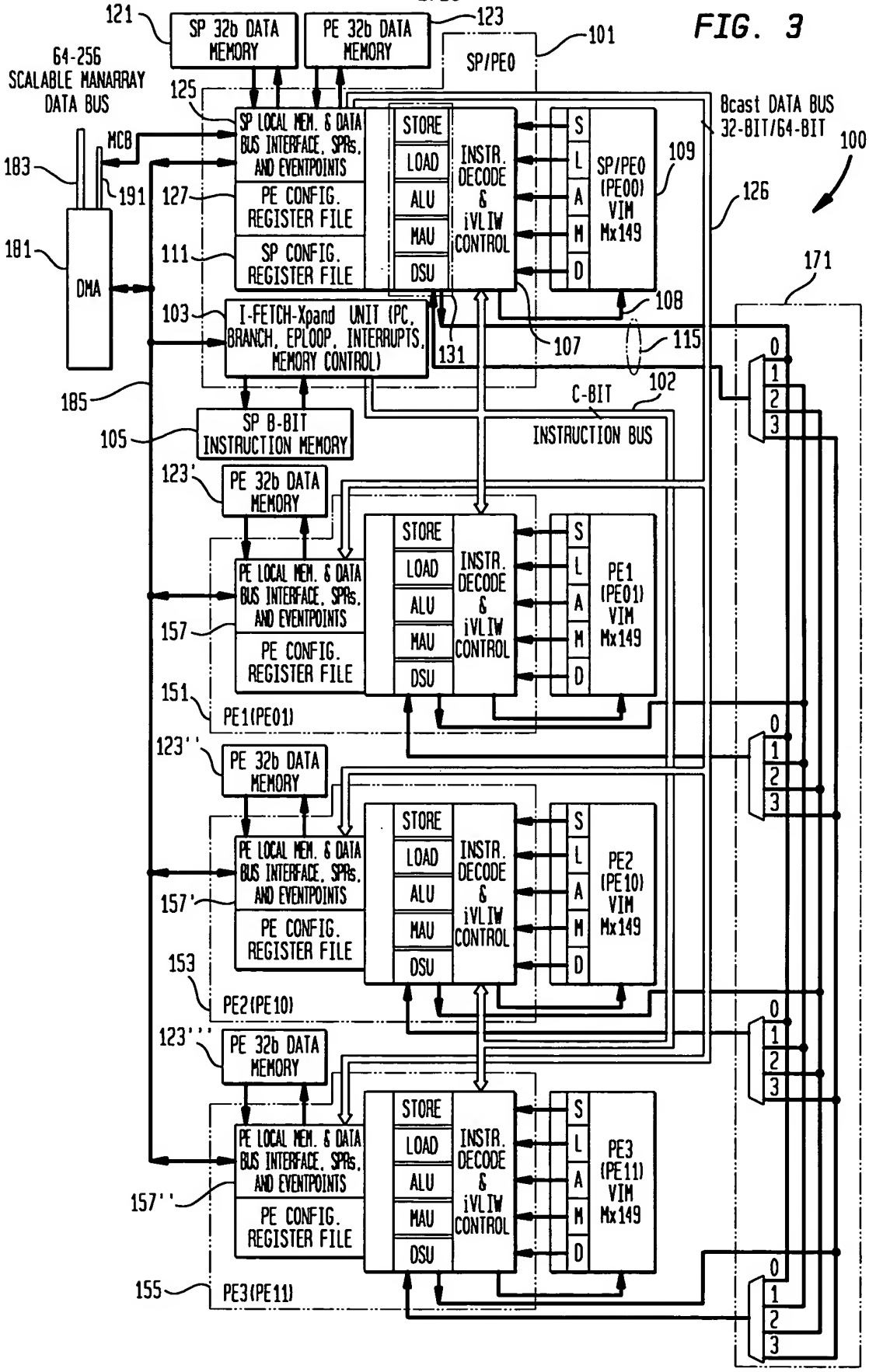
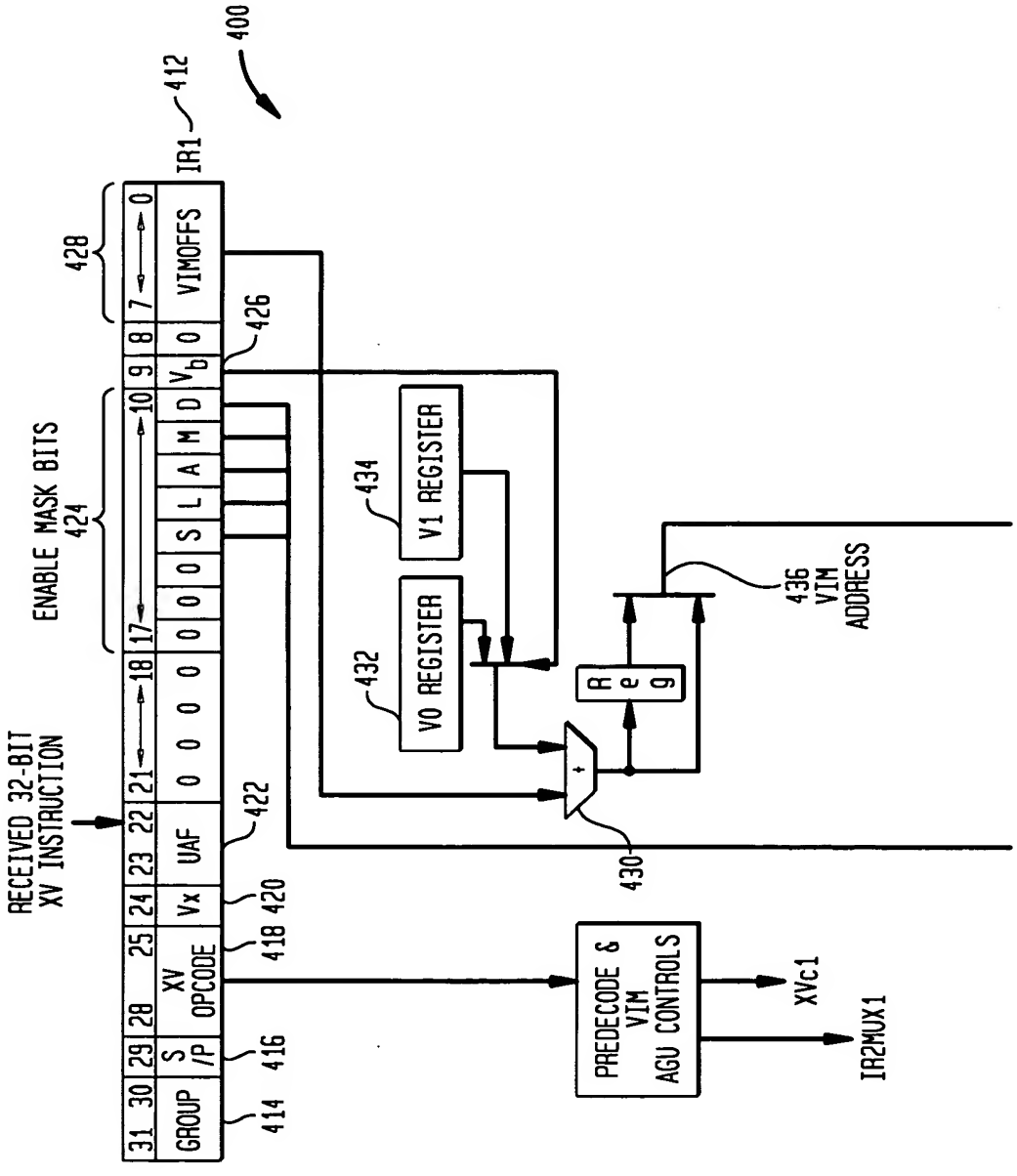

121
SP 32b DATA MEMORY
123
PE 32b DATA MEMORY
101
SP/PE0
64-256 SCALABLE MANARRAY DATA BUS
125
SP LOCAL MEM. & DATA BUS INTERFACE, SPRs, AND EVENTPOINTS
STORE
LOAD
ALU
MAU
DSU
INSTR. DECODE & iVLIW CONTROL
S
L
A
M
D
SP/PE0 (PE00) VIM Mx149
109
Bcast DATA BUS 32-BIT/64-BIT
100
MCB
183
191
127
PE CONFIG. REGISTER FILE
126
181
DMA
111
SP CONFIG. REGISTER FILE
171
103
I-FETCH-Xpand UNIT (PC, BRANCH, EPLOOP, INTERRUPTS, MEMORY CONTROL)
131
107
108
115
185
C-BIT
102
105
SP 8-BIT INSTRUCTION MEMORY
INSTRUCTION BUS
123'
PE 32b DATA MEMORY
PE LOCAL MEM. & DATA BUS INTERFACE, SPRs, AND EVENTPOINTS
157
PE CONFIG. REGISTER FILE
PE1 (PE01) VIM Mx149
151
PE1(PE01)
123''
PE 32b DATA MEMORY
PE LOCAL MEM. & DATA BUS INTERFACE, SPRs, AND EVENTPOINTS
157'
PE CONFIG. REGISTER FILE
PE2 (PE10) VIM Mx149
153
PE2(PE10)
123'''
PE 32b DATA MEMORY
PE LOCAL MEM. & DATA BUS INTERFACE, SPRs, AND EVENTPOINTS
157''
PE CONFIG. REGISTER FILE
PE3 (PE11) VIM Mx149
155
PE3(PE11)
0
1
2
3

FIG. 4A


400
412
IR1
428
426
424
ENABLE MASK BITS
RECEIVED 32-BIT XV INSTRUCTION
422
420
418
416
414
GROUP
S /P
XV OPCODE
Vx
UAF
VIMOFFS
V_b
D
M
A
L
S
0
0 0 0 0 0
31 30 29 28 25 24 23 22 21 18 17 10 9 8 7 0
V0 REGISTER
432
V1 REGISTER
434
Reg
430
436
VIM ADDRESS
PREDECODE & VIM AGU CONTROLS
XVc1
IR2MUX1

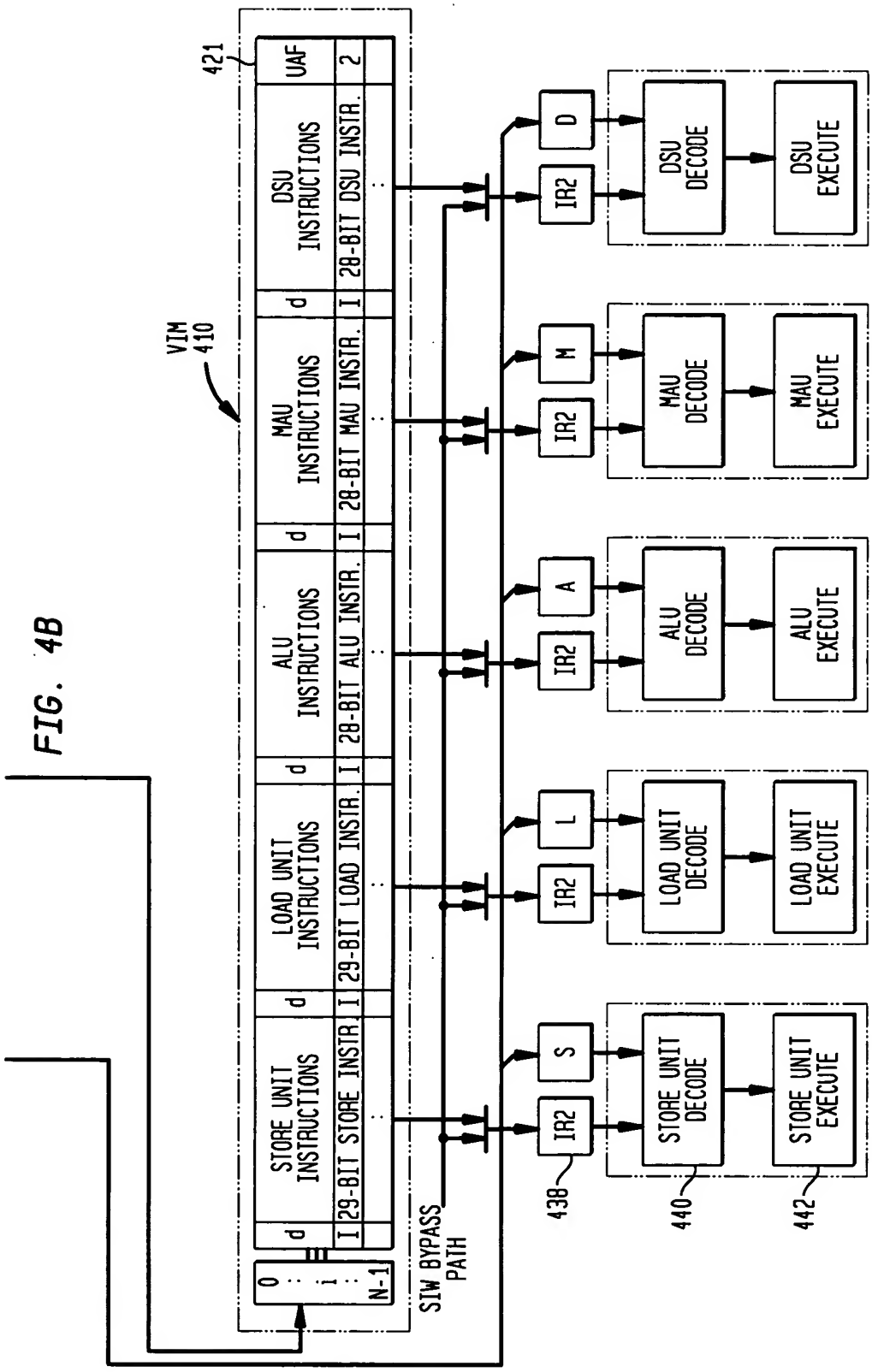
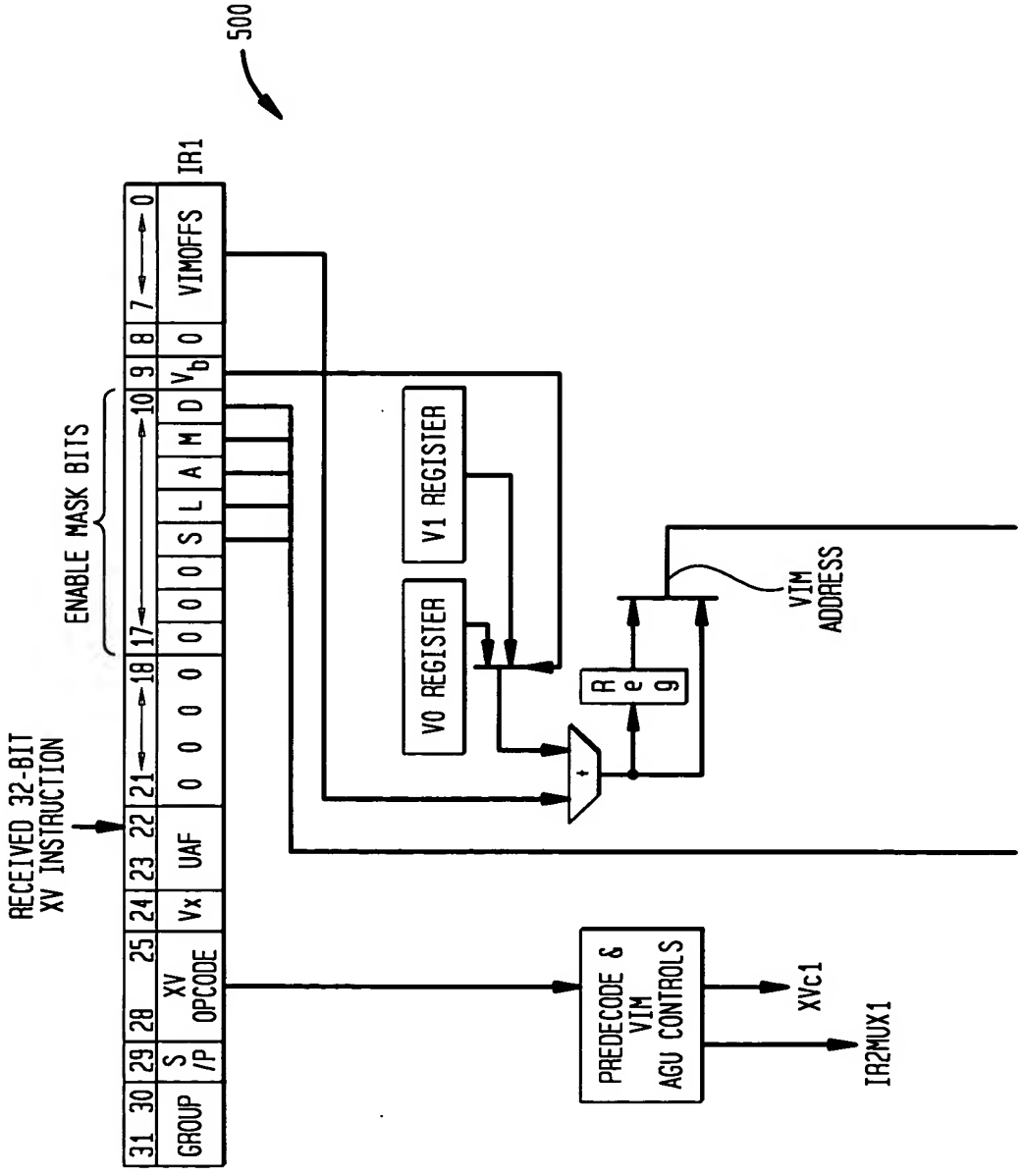

VIM
410
421
STORE UNIT INSTRUCTIONS
d
I
29-BIT STORE INSTR.
LOAD UNIT INSTRUCTIONS
29-BIT LOAD INSTR.
ALU INSTRUCTIONS
28-BIT ALU INSTR.
MAU INSTRUCTIONS
28-BIT MAU INSTR.
DSU INSTRUCTIONS
28-BIT DSU INSTR.
UAF
2
0
i
N-1
SIW BYPASS PATH
S
L
A
M
D
IR2
438
STORE UNIT DECODE
LOAD UNIT DECODE
ALU DECODE
MAU DECODE
DSU DECODE
440
STORE UNIT EXECUTE
LOAD UNIT EXECUTE
ALU EXECUTE
MAU EXECUTE
DSU EXECUTE
442

FIG. 4B

FIG. 5A


500
IR1
RECEIVED 32-BIT XV INSTRUCTION
ENABLE MASK BITS
31 30 29 28 25 24 23 22 21 18 17 10 9 8 7 0
GROUP
S /P
XV OPCODE
Vx
UAF
0 0 0 0 0
0 0 0 S L A M D
V_b 0
VIMOFFS
V0 REGISTER
V1 REGISTER
+
Reg
VIM ADDRESS
PREDECODE & VIM AGU CONTROLS
XVc1
IR2MUX1

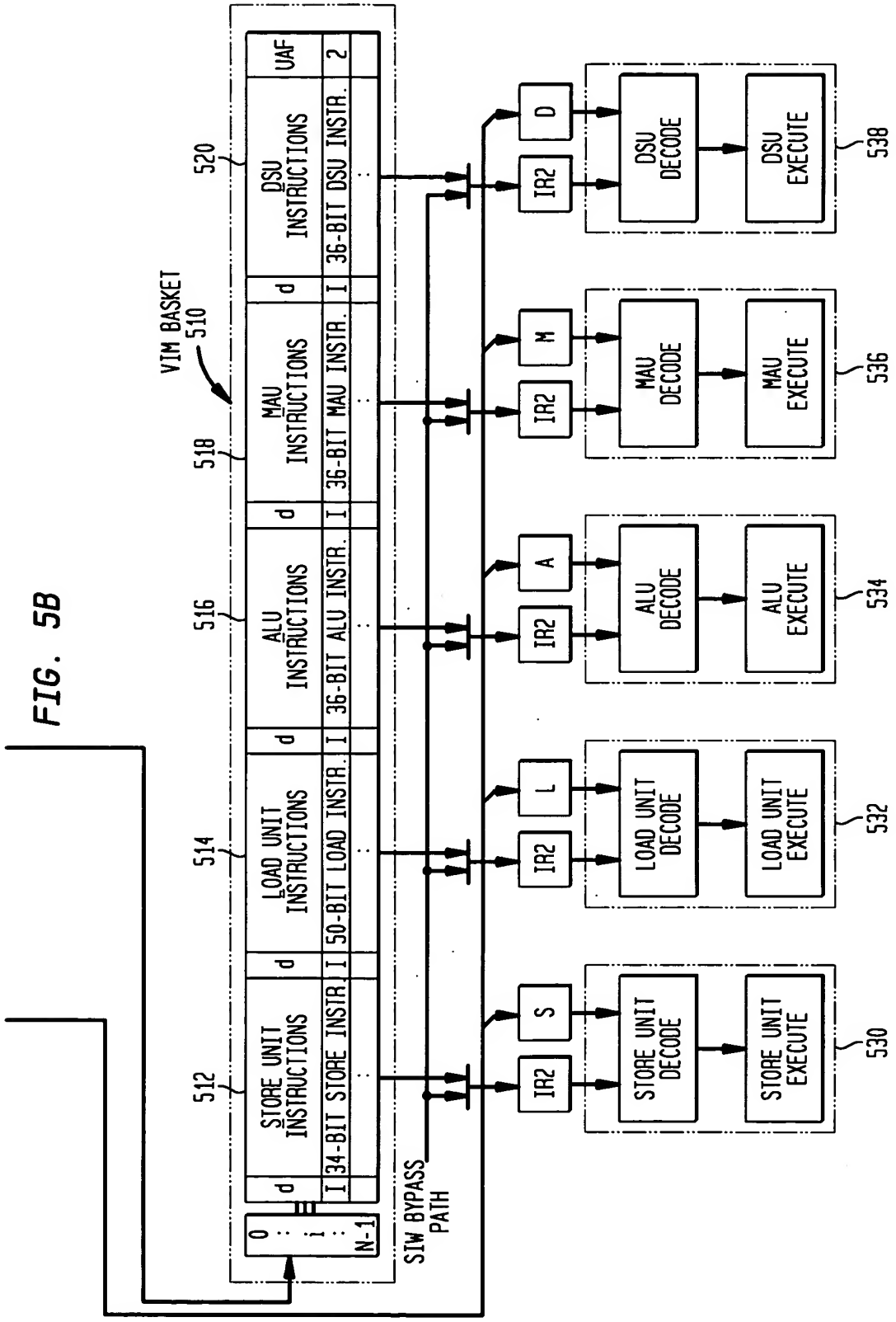

VIM BASKET
510
512
STORE UNIT INSTRUCTIONS
34-BIT STORE INSTR.
514
LOAD UNIT INSTRUCTIONS
50-BIT LOAD INSTR.
516
ALU INSTRUCTIONS
36-BIT ALU INSTR.
518
MAU INSTRUCTIONS
36-BIT MAU INSTR.
520
DSU INSTRUCTIONS
36-BIT DSU INSTR.
UAF
d
I
0
i
N-1
SIW BYPASS PATH
IR2
S
L
A
M
D
STORE UNIT DECODE
STORE UNIT EXECUTE
LOAD UNIT DECODE
LOAD UNIT EXECUTE
ALU DECODE
ALU EXECUTE
MAU DECODE
MAU EXECUTE
DSU DECODE
DSU EXECUTE
530
532
534
536
538

FIG. 5B

FIG. 6A
(PRIOR ART)

32-bit Encoding

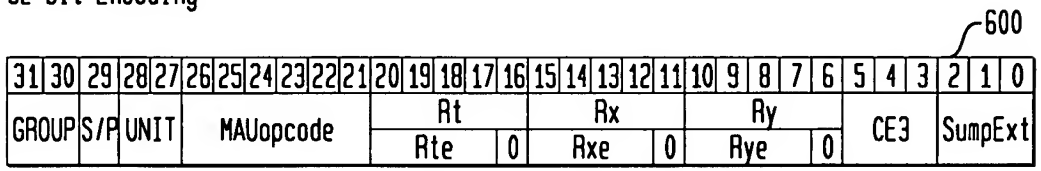


FIG. 6B

SLAMDunk 40-bit Encoding Example

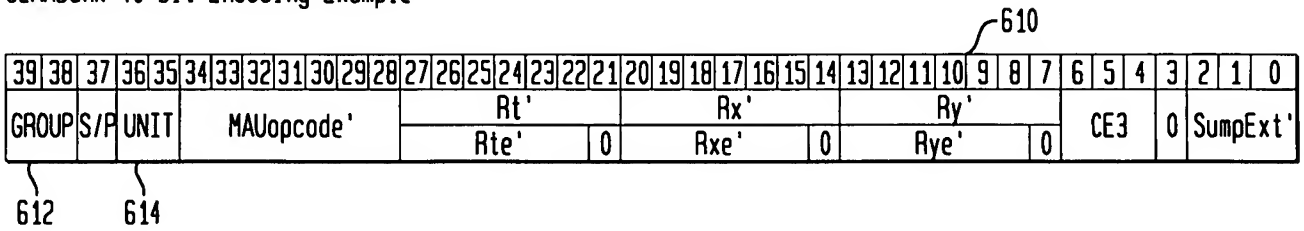


FIG. 6C

32-bit Mapping to SLAMDunk 40-bit Encoding Example

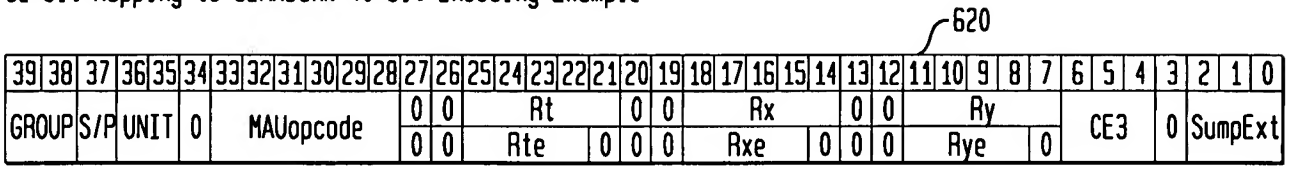


FIG. 7A

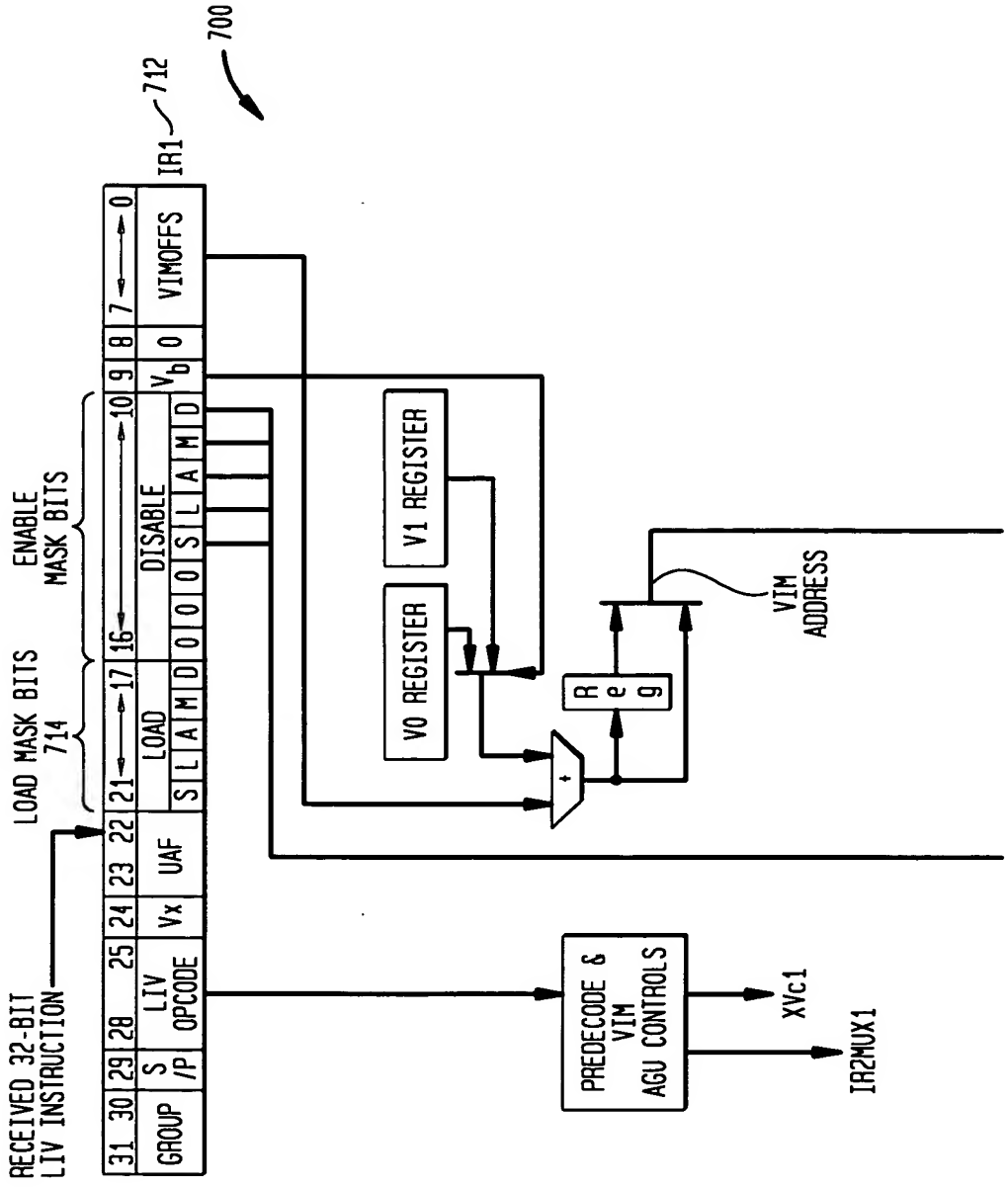

700
712
IR1
RECEIVED 32-BIT LIV INSTRUCTION
LOAD MASK BITS 714
ENABLE MASK BITS
31 30 29 28 25 24 23 22 21 17 16 10 9 8 7 0
GROUP
S /P
LIV OPCODE
Vx
UAF
LOAD
DISABLE
S L A M D 0 0 0 S L A M D
V_b
0
VIMOFFS
V0 REGISTER
V1 REGISTER
+
R e g
VIM ADDRESS
PREDECODE & VIM AGU CONTROLS
XVc1
IR2MUX1

FIG. 7B

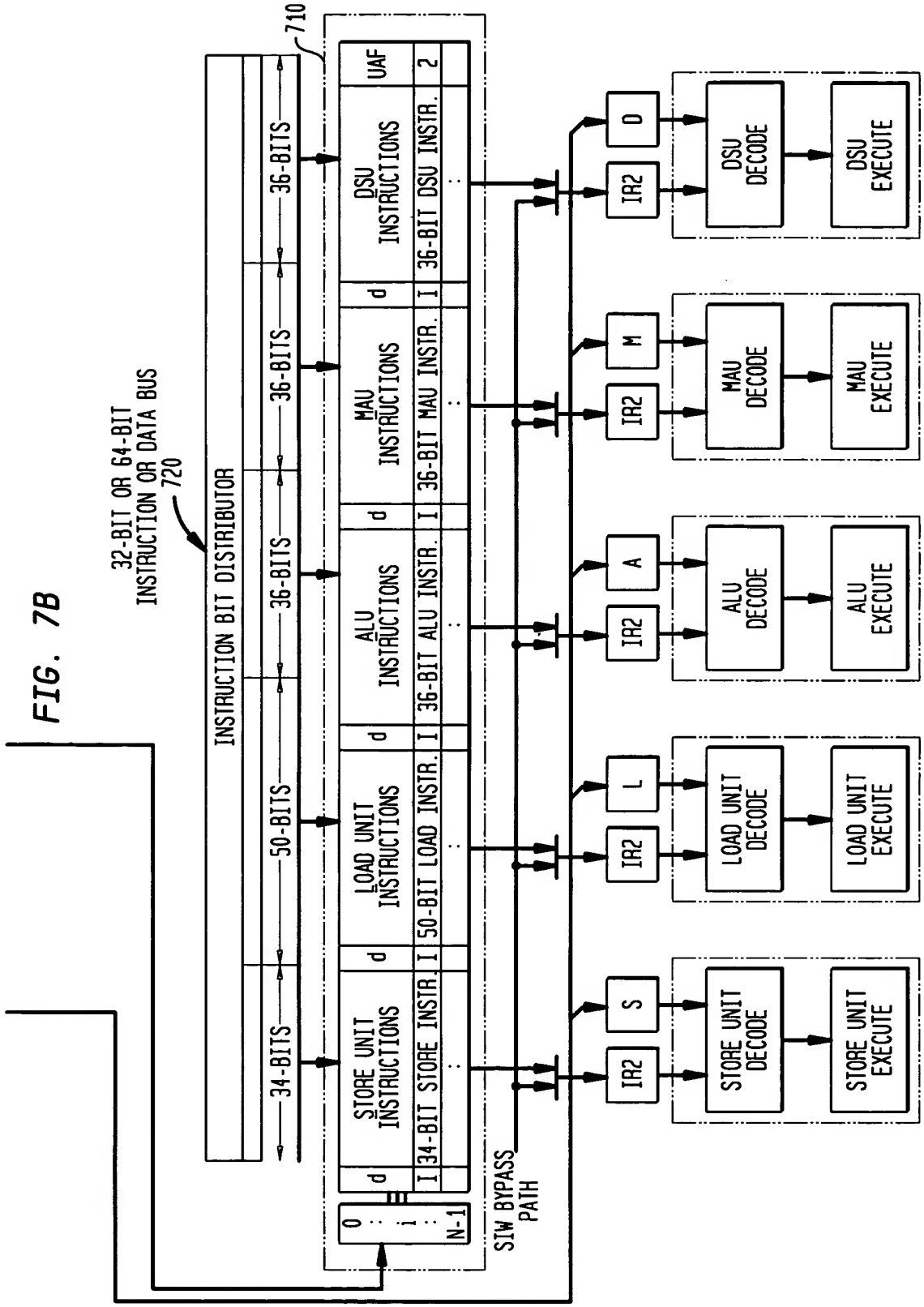
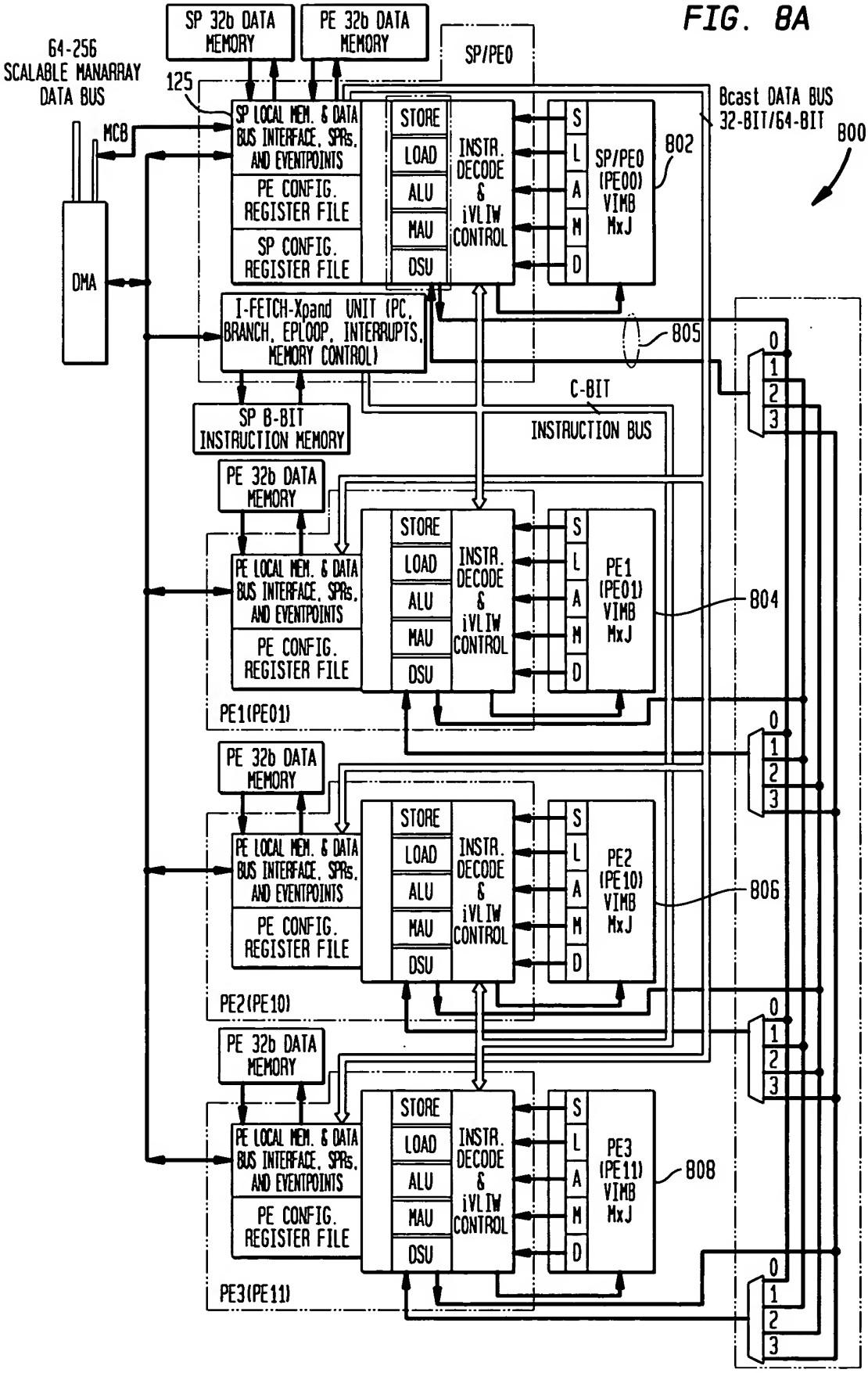

32-BIT OR 64-BIT
INSTRUCTION OR DATA BUS
720
INSTRUCTION BIT DISTRIBUTOR
34-BITS
50-BITS
36-BITS
36-BITS
36-BITS
710
STORE UNIT INSTRUCTIONS
LOAD UNIT INSTRUCTIONS
ALU INSTRUCTIONS
MAU INSTRUCTIONS
DSU INSTRUCTIONS
UAF
d
I
34-BIT STORE INSTR.
50-BIT LOAD INSTR.
36-BIT ALU INSTR.
36-BIT MAU INSTR.
36-BIT DSU INSTR.
2
0
i
N-1
SIW BYPASS PATH
IR2
S
L
A
M
D
STORE UNIT DECODE
LOAD UNIT DECODE
ALU DECODE
MAU DECODE
DSU DECODE
STORE UNIT EXECUTE
LOAD UNIT EXECUTE
ALU EXECUTE
MAU EXECUTE
DSU EXECUTE

FIG. 8A


SP 32b DATA MEMORY
PE 32b DATA MEMORY
SP/PE0
64-256 SCALABLE MANARRAY DATA BUS
125
Bcast DATA BUS 32-BIT/64-BIT
800
MCB
DMA
SP LOCAL MEM. & DATA BUS INTERFACE, SPRs, AND EVENTPOINTS
PE CONFIG. REGISTER FILE
SP CONFIG. REGISTER FILE
STORE
LOAD
ALU
MAU
DSU
INSTR. DECODE & iVLIW CONTROL
S
L
A
M
D
SP/PE0 (PE00) VIMB MxJ
802
I-FETCH-Xpand UNIT (PC, BRANCH, EPLOOP, INTERRUPTS, MEMORY CONTROL)
805
C-BIT
INSTRUCTION BUS
SP B-BIT INSTRUCTION MEMORY
PE LOCAL MEM. & DATA BUS INTERFACE, SPRs, AND EVENTPOINTS
PE CONFIG. REGISTER FILE
PE1 (PE01) VIMB MxJ
804
PE1(PE01)
PE2 (PE10) VIMB MxJ
806
PE2(PE10)
PE3 (PE11) VIMB MxJ
808
PE3(PE11)
0
1
2
3

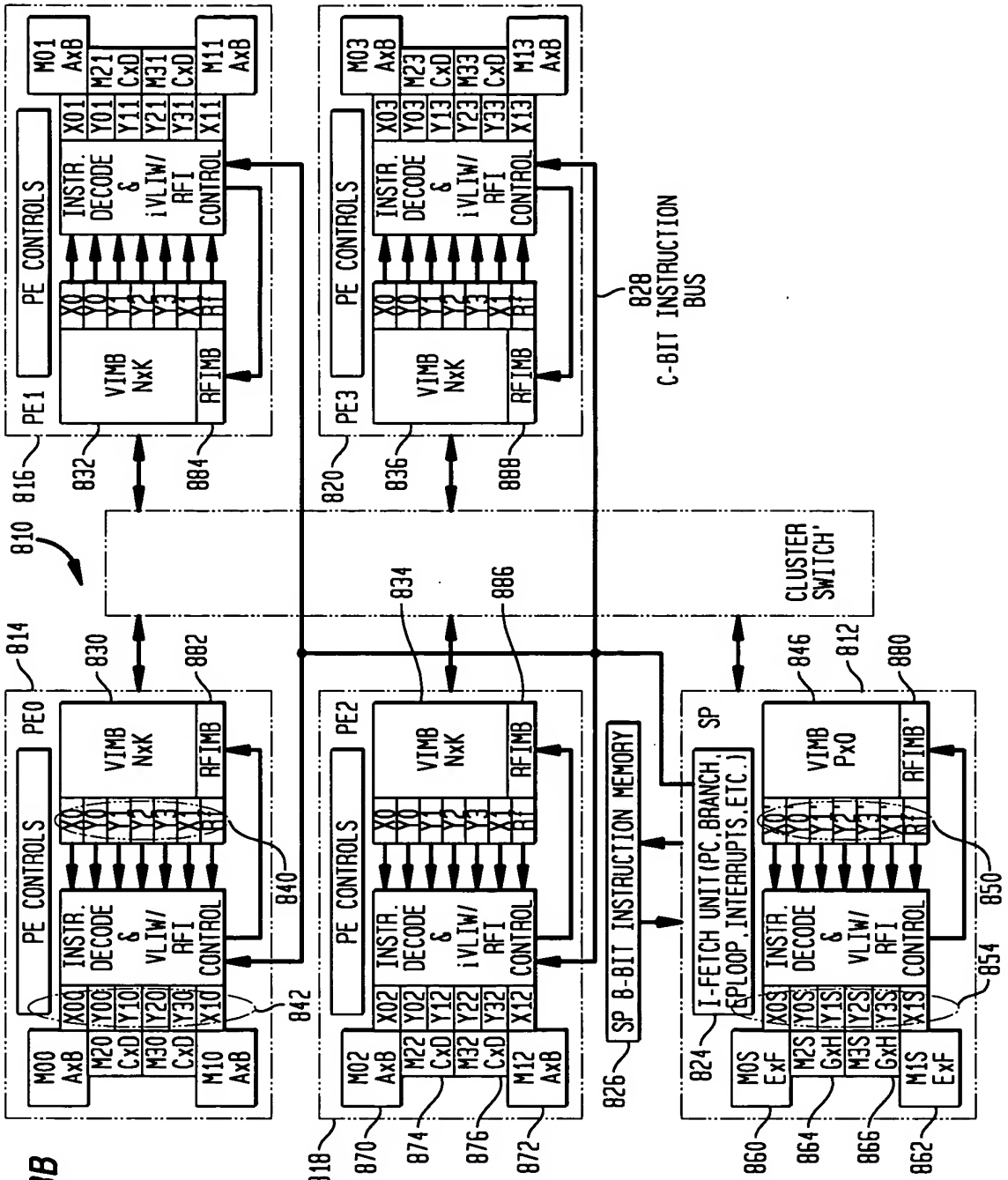

PE0
PE1
PE2
PE3
SP
PE CONTROLS
VIMB NxK
RFIMB
INSTR. DECODE & VLIW/ RFI CONTROL
VIMB PxO
RFIMB'
I-FETCH UNIT(PC,BRANCH, &PLOOP,INTERRUPTS,ETC.)
SP 8-BIT INSTRUCTION MEMORY
C-BIT INSTRUCTION BUS
828
CLUSTER SWITCH'
810
812
814
816
818
820
824
826
830
832
834
836
840
842
846
850
854
860
862
864
866
870
872
874
876
880
882
884
886
888
M00 AxB
M01 AxB
M02 AxB
M03 AxB
M05 ExF
M10 AxB
M11 AxB
M12 AxB
M13 AxB
M1S ExF
M20 CxD
M21 CxD
M22 CxD
M23 CxD
M2S GxH
M30 CxD
M31 CxD
M32 CxD
M33 CxD
M3S GxH
X00
X01
X02
X03
X0S
X10
X11
X12
X13
X1S
Y00
Y01
Y02
Y03
Y0S
Y10
Y11
Y12
Y13
Y1S
Y20
Y21
Y22
Y23
Y2S
Y30
Y31
Y32
Y33
Y3S
X0
Y0
Y1
Y2
Y3
X1
R1
R7

FIG. 8B

FIG. 9A

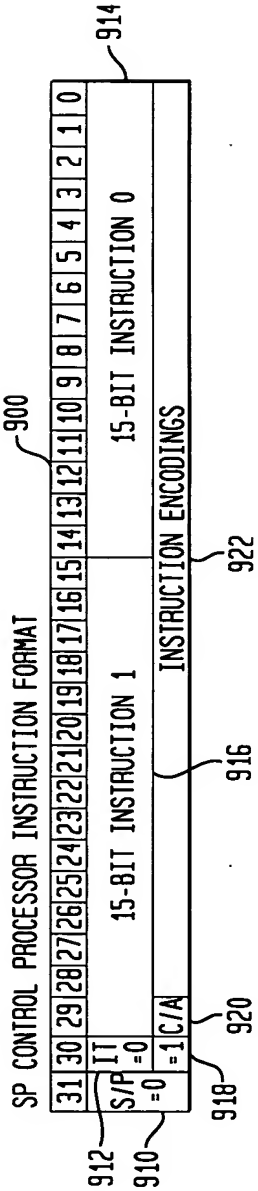

SP CONTROL PROCESSOR INSTRUCTION FORMAT
900
914
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
S/P =0
IT =0
15-BIT INSTRUCTION 1
15-BIT INSTRUCTION 0
=1
C/A
INSTRUCTION ENCODINGS
912
910
918
920
916
922

FIG. 9B

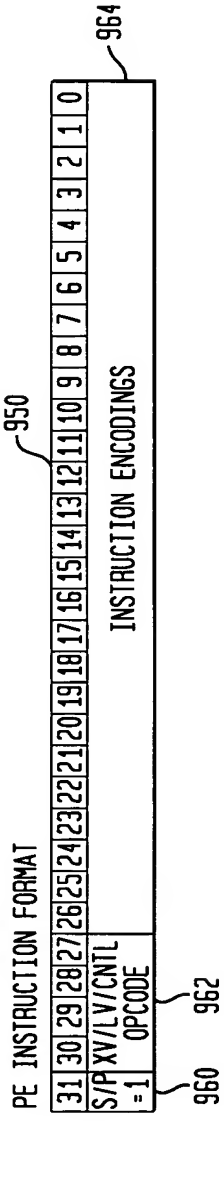

PE INSTRUCTION FORMAT
950
964
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
S/P =1
XV/LV/CNTL
OPCODE
INSTRUCTION ENCODINGS
960
962

FIG. 10A

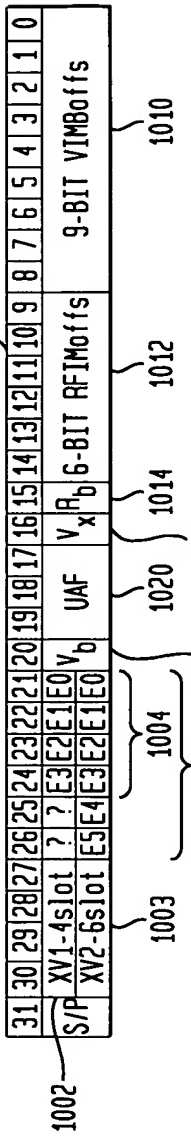


FIG. 10B

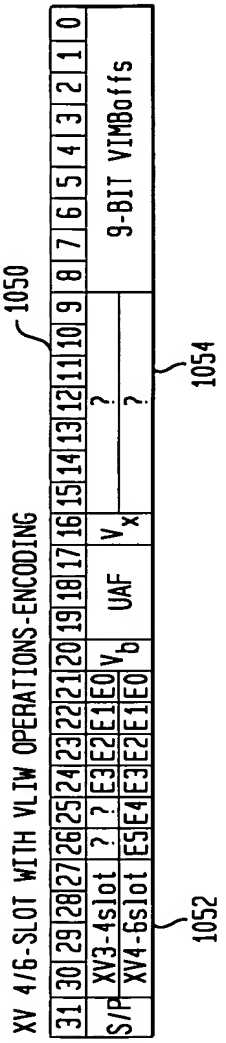


FIG. 11A

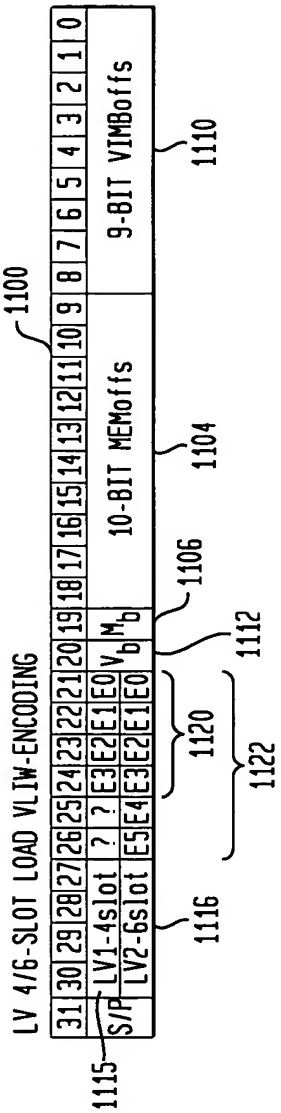


FIG. 11B

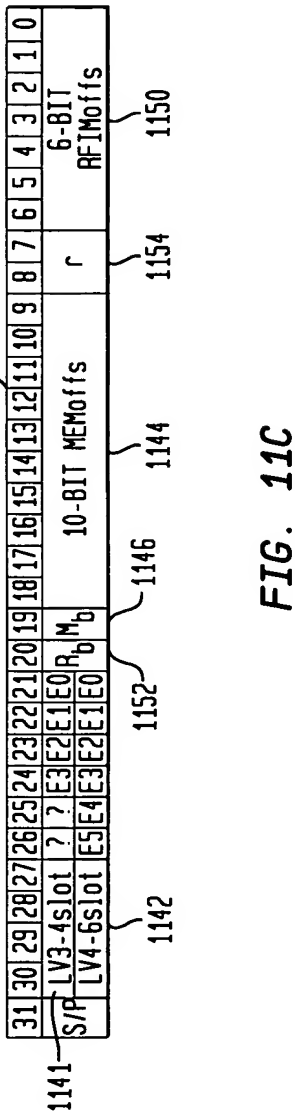


FIG. 11C

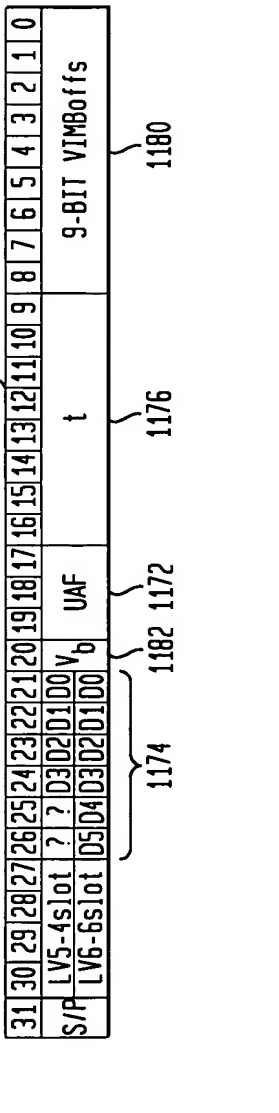
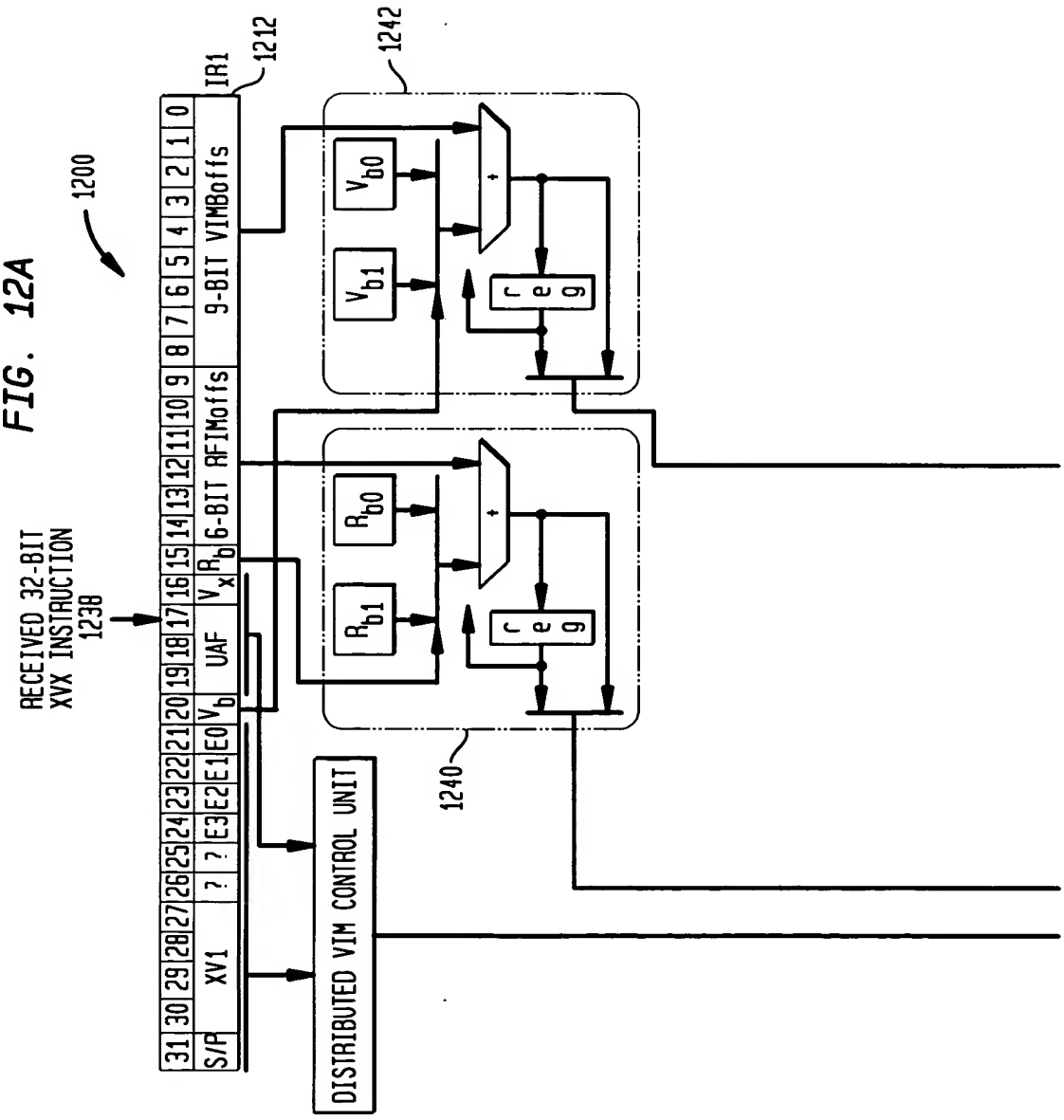


FIG. 12A


1200
1212
1242
1240
1238
IR1
RECEIVED 32-BIT
XVX INSTRUCTION
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
S/A
XV1
?
?
E3 E2 E1 E0
Vb
UAF
Vx
Rb
6-BIT AFIMoffs
9-BIT VIMBoffs
Vb0
Vb1
Rb0
Rb1
reg
DISTRIBUTED VIM CONTROL UNIT

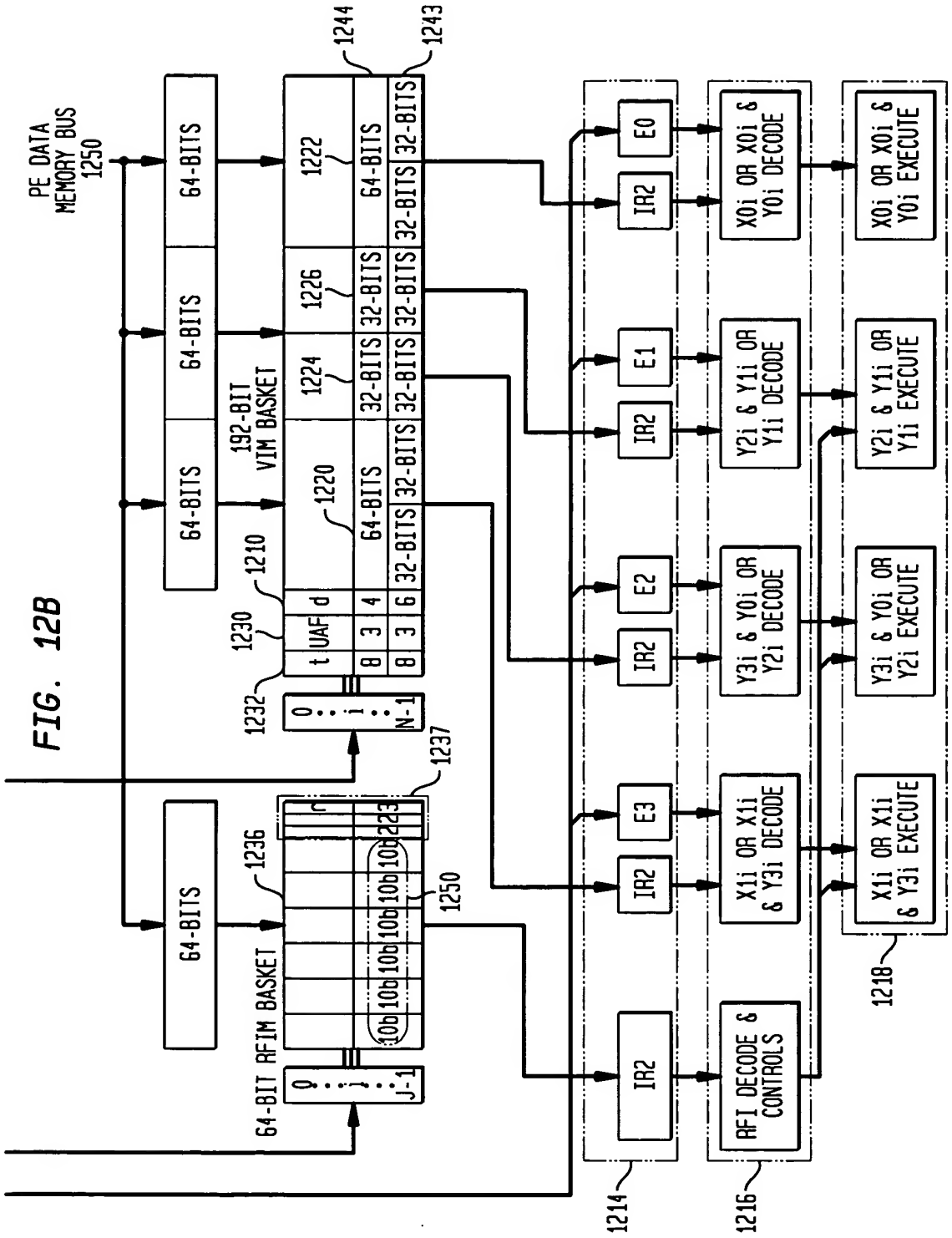
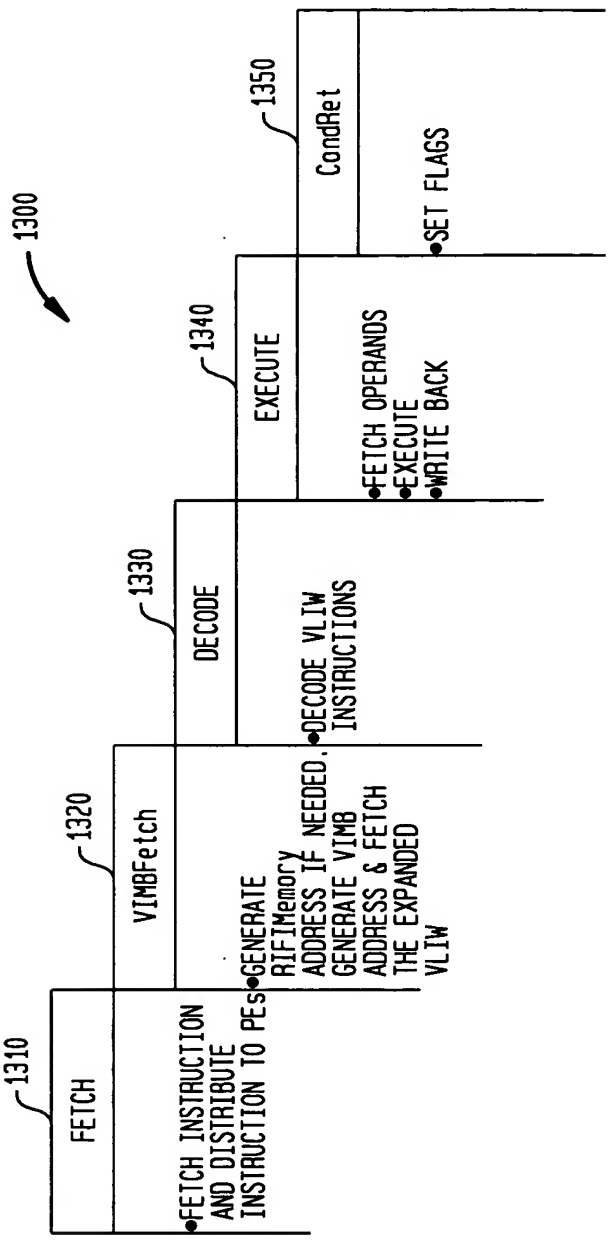

PE DATA MEMORY BUS 1250
64-BITS
64-BITS
64-BITS
64-BITS
192-BIT VIM BASKET
1222
1226
1224
1220
1244
1243
64-BITS
32-BITS
32-BITS
32-BITS
32-BITS
32-BITS
32-BITS
32-BITS
t UAF d
8 3 4 6
8 3 6
1210
1230
1232
0 i N-1
1237
64-BIT RFIM BASKET
1236
1250
10b 10b 10b 10b 10b 10b
J-1
IR2
E3
E2
E1
E0
X1i OR X1i & Y3i DECODE
Y3i & Y0i OR Y2i DECODE
Y2i & Y1i OR Y1i DECODE
X0i OR X0i & Y0i DECODE
X1i OR X1i & Y3i EXECUTE
Y3i & Y0i OR Y2i EXECUTE
Y2i & Y1i OR Y1i EXECUTE
X0i OR X0i & Y0i EXECUTE
RFI DECODE & CONTROLS
1214
1216
1218

FIG. 12B

FIG. 13


1300
1310
FETCH
•FETCH INSTRUCTION AND DISTRIBUTE INSTRUCTION TO PEs
1320
VIMBFetch
•GENERATE RIFIMemory ADDRESS IF NEEDED.
GENERATE VIMB ADDRESS & FETCH THE EXPANDED VLIW
1330
DECODE
•DECODE VLIW INSTRUCTIONS
1340
EXECUTE
•FETCH OPERANDS
•EXECUTE
•WRITE BACK
1350
CondRet
•SET FLAGS

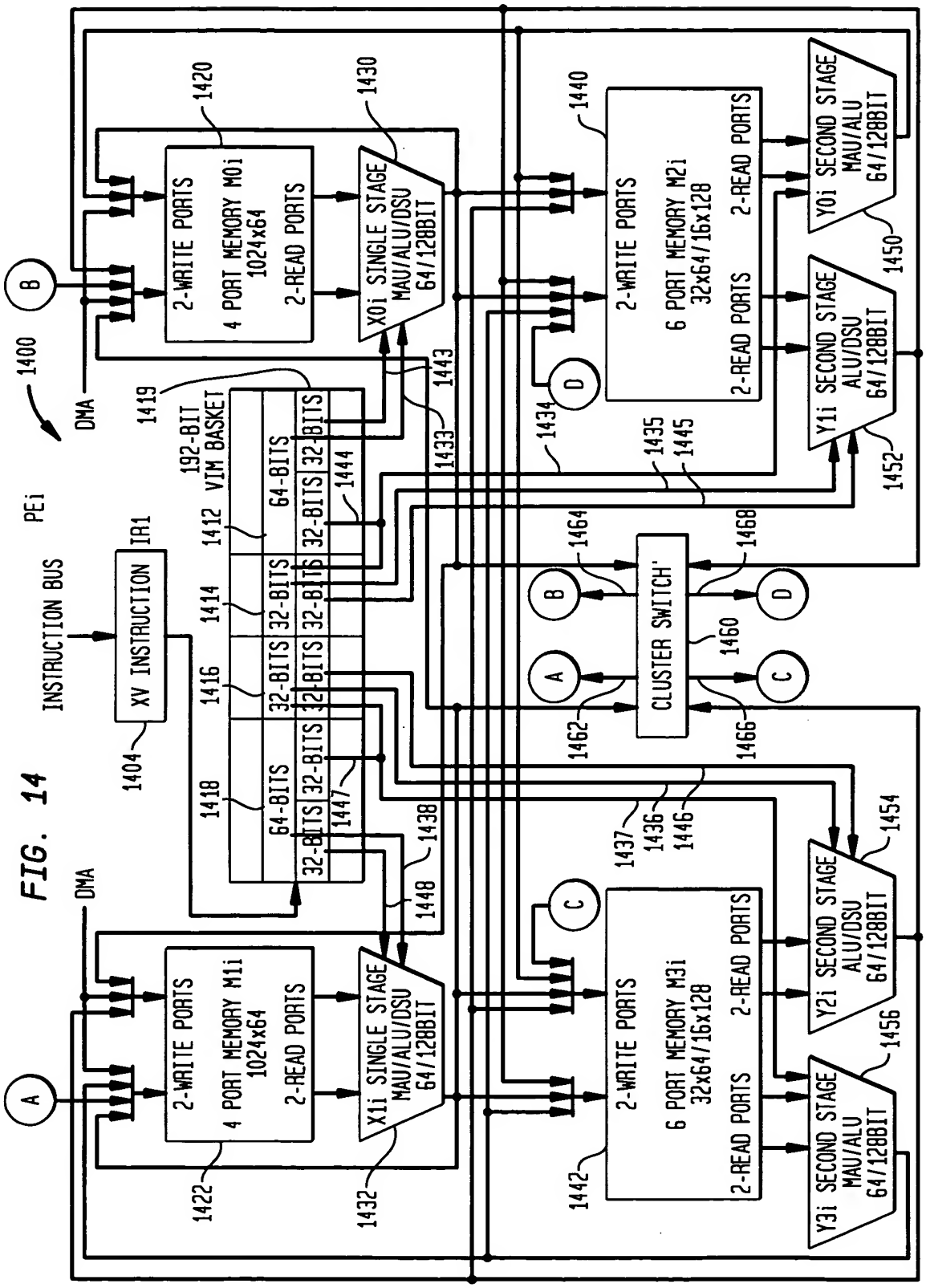

PEi
1400
INSTRUCTION BUS
DMA
IR1
XV INSTRUCTION
1404
192-BIT VIM BASKET
1412
1414
1416
1418
64-BITS
32-BITS
1419
1420
2-WRITE PORTS
4 PORT MEMORY M0i 1024x64
2-READ PORTS
1422
1430
X0i SINGLE STAGE MAU/ALU/DSU 64/128BIT
1432
1433
1434
1435
1436
1437
1438
1440
2-WRITE PORTS
6 PORT MEMORY M2i 32x64/16x128
2-READ PORTS
1442
1443
1444
1445
1446
1447
1448
1450
Y0i SECOND STAGE MAU/ALU 64/128BIT
Y1i SECOND STAGE ALU/DSU 64/128BIT
1452
1454
Y2i SECOND STAGE ALU/DSU 64/128BIT
1456
Y3i SECOND STAGE MAU/ALU 64/128BIT
CLUSTER SWITCH'
1460
1462
1464
1466
1468
A
B
C
D

FIG. 14

FIG. 15

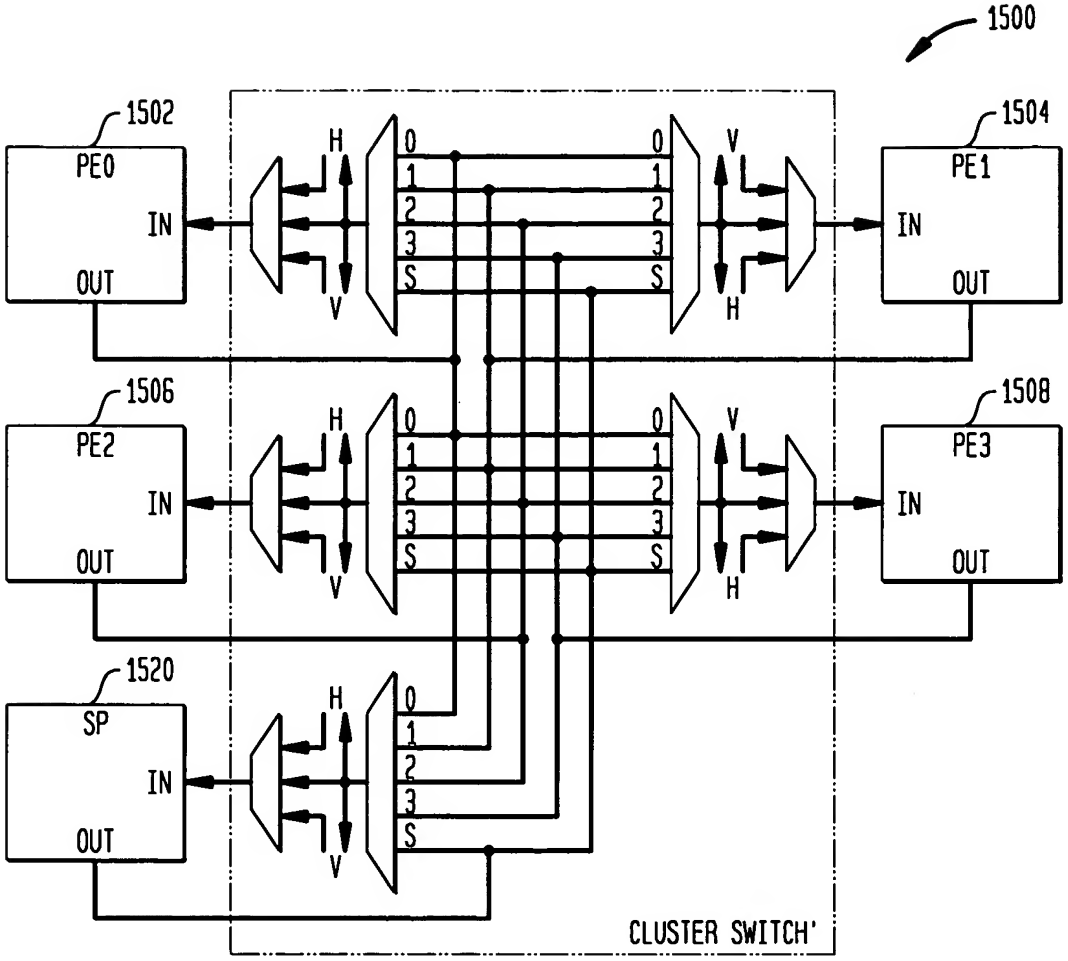

1500
1502
PE0
IN
OUT
1504
PE1
IN
OUT
1506
PE2
IN
OUT
1508
PE3
IN
OUT
1520
SP
IN
OUT
H
V
0
1
2
3
S
CLUSTER SWITCH'

FIG. 16

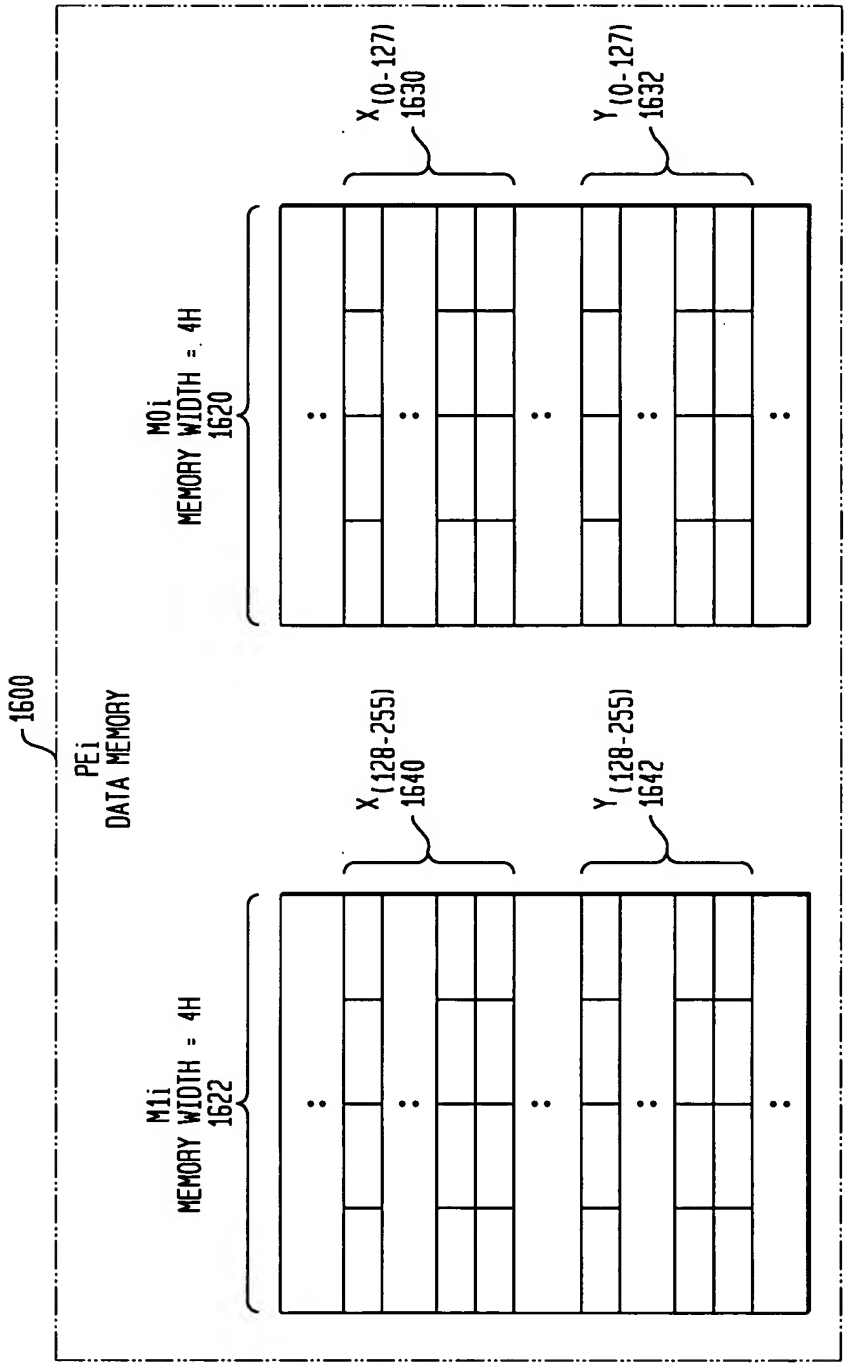

1600
PEi
DATA MEMORY
M0i
MEMORY WIDTH = 4H
1620
X(0-127)
1630
Y(0-127)
1632
M1i
MEMORY WIDTH = 4H
1622
X(128-255)
1640
Y(128-255)
1642

FIG. 17

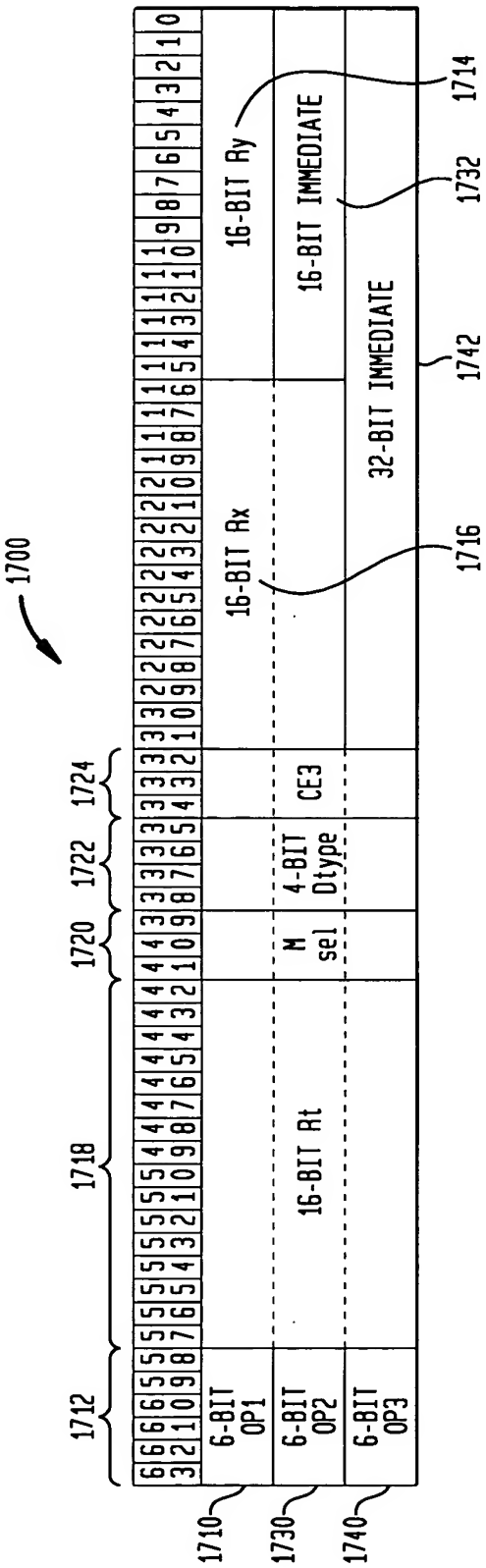

1700
1712
1718
1720
1722
1724
6-BIT OP1
6-BIT OP2
6-BIT OP3
16-BIT Rt
M sel
4-BIT Dtype
CE3
16-BIT Rx
16-BIT Ry
16-BIT IMMEDIATE
32-BIT IMMEDIATE
1710
1730
1740
1714
1716
1732
1742

FIG. 18

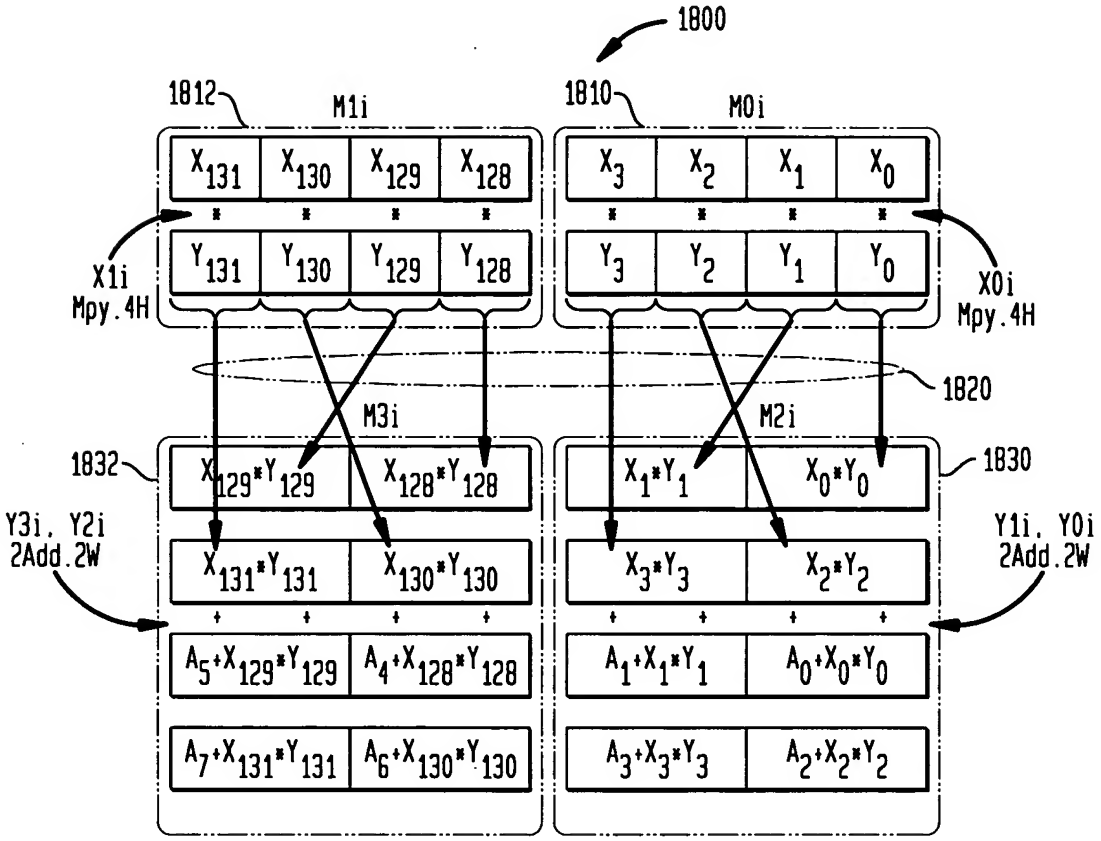
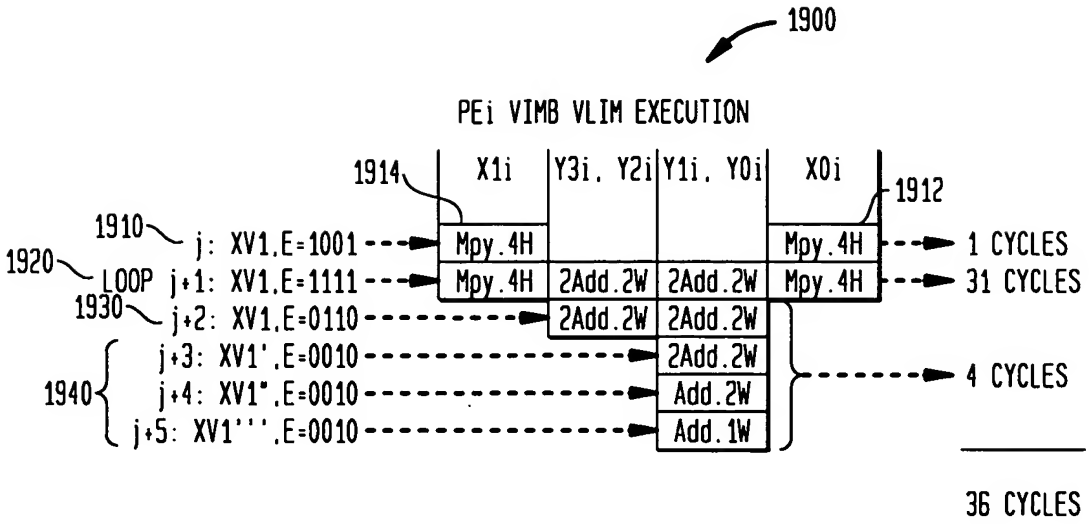

1800
1812
M1i
1810
M0i
X131 X130 X129 X128
Y131 Y130 Y129 Y128
X3 X2 X1 X0
Y3 Y2 Y1 Y0
X1i
Mpy.4H
X0i
Mpy.4H
1820
M3i
M2i
1832
1830
X129*Y129 X128*Y128
X131*Y131 X130*Y130
X1*Y1 X0*Y0
X3*Y3 X2*Y2
Y3i, Y2i
2Add.2W
Y1i, Y0i
2Add.2W
A5+X129*Y129 A4+X128*Y128
A7+X131*Y131 A6+X130*Y130
A1+X1*Y1 A0+X0*Y0
A3+X3*Y3 A2+X2*Y2

FIG. 19


1900
PEi VIMB VLIM EXECUTION
1914
X1i
Y3i, Y2i
Y1i, Y0i
X0i
1912
1910
j: XV1,E=1001
Mpy.4H
Mpy.4H
1 CYCLES
1920
LOOP j+1: XV1,E=1111
Mpy.4H
2Add.2W
2Add.2W
Mpy.4H
31 CYCLES
1930
j+2: XV1,E=0110
2Add.2W
2Add.2W
1940
j+3: XV1',E=0010
2Add.2W
j+4: XV1",E=0010
Add.2W
j+5: XV1''',E=0010
Add.1W
4 CYCLES
36 CYCLES